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SEMICONDUCTOR DEVICE PACKAGE DIEPAD HAVING FEATURES FORMED BY ELECTROPLATING

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BACKGROUND OF THE INVENTION

[0001] Figure 1A shows an underside plan view of a conventional quad flat no-lead (QFN) package utilized to house a semiconductor device. Figure 1B shows a cross-sectional view taken along line B-B', of the conventional QFN package of Figure 1A, positioned on a PC board.

[0002] QFN package 100 comprises semiconductor die 102 having electrically active structures fabricated thereon. Die 102 is affixed to underlying diepad 104a portion of lead frame 104 by adhesive 106. The relative thickness of the die and lead frame shown in Figure 1B, and all other drawings of this patent application, is not to scale. Lead frame 104 also comprises non-integral pin portions 104b in electrical communication with die 102 through bond wires 108. Bond wires 108 also allow electrical communication between die 102 and diepad 104a.

[0003] Plastic molding 109 encapsulates all but the exposed portions 104a' and 104b' of the lead frame portions 104a and 104b, respectively. For the purposes of this patent application, the term "encapsulation" refers to partial or total enveloping of an element in a surrounding material, typically the metal of the lead frame within a surrounding dielectric material such as plastic.

[0004] Portions of the upper surface of lead frame 104 bear silver Ag 105 formed by electroplating. The lower surface of lead frame 104 bears a layer of Pd/Ni or Au/Ni 107 formed by electroplating.

[0005] QFN package 100 is secured to traces 110 of underlying PC board 112 by solder 114 that preferably has the rounded shape indicated. The electrically conducting properties of solder 114 allows electrical signals to pass between lead frame portions 104a and 104b and the underlying traces 110.

[0006] Figure 1C shows a plan view of only the lead-frame 104 of QFN package 100 of Figures 1A-B. Lead frame 104 is typically formed by etching a pattern of holes completely through a uniform sheet of copper. Figure 1D shows one example of such a pattern of holes 116 in a copper roll 118. These patterns of holes define a proto-lend

frame 122 comprising proto-diepad 124 and proto-non-integral portions 126. Proto-diepad 124 is secured to the surrounding metal frame by tie bars 120. Proto-non-integral pin portions 126 are secured to the surrounding metal frame by tabs 128.

[0007] The patterned metal portion shown in Figure 1D is processed into a package by gluing a die to the diepad, and connecting bond wires between the die and non-integral portions and/or the diepad. While the diepad and non-integral portions are still attached to the surrounding metal, the bond wires and a portion of the diepad and non-integral lead frame portions are encapsulated within a dielectric material such as plastic. Fabrication of an individual package is then completed by severing the tabs and tie bars to singulate an individual package from its surrounding metal frame and other packages associated therewith.

[0008] While adequate for many purposes, the conventional QFN package just described offers some drawbacks. One drawback is the difficulty of forming raised features on the lead frame.

[0009] For example, Figure 1B shows that non-integral lead frame pin portions 104b exhibit a thinned region 104b" proximate to the diepad. Thinned pin region 104b" is surrounded on three sides by the plastic encapsulant 109 of the package body, thereby physically securing non-integral pin portion 104b within the package.

[0010] Moreover, Figure 1B also shows that diepad portions 104a exhibit a thinned region 104a" proximate to the non-integral pins. Thinned diepad region 104a" is surrounded on three sides by the plastic encapsulant of the package body, thereby physically securing the diepad within the package.

[0011] Figures 1E - 1H show cross-sectional views of the conventional process steps for fabricating a lead frame having a thinned portion. In Figure 1E, the inverted Cu sheet 118 is electroplated on its bottom surface with an Au/Pd/Ni combination or an Ag/Ni combination to form layer 107. For the Au/Pd/Ni combination, the Au is between about 0.01-0.015 μm in thickness, the Pd is between about 0.02-0.2 μm in thickness, and the Ni is between about 0.5-2.5 μm in thickness. For an Ag/Ni electroplated coating, Ag and Ni are each between about 0.5-2.5 μm in thickness.

[0012] In Figure 1F, photoresist mask 150 is patterned over layer 107 to expose the regions 152 that are to be thinned. Exposed regions 152 are then exposed to an etchant for a controlled period, which removes Cu material to a predetermined depth Y.

[0013] In Figure 1G, the photoresist mask is removed, and Cu roll 118 is then reoriented right side up. The upper surface of the Cu roll 118 is then selectively electroplated to form silver layer 105. The silver may be electroplated only in specific regions over the substrate utilizing a mask (not shown) during this step.

[0014] In Figure 1H, the backside of partially-etched Cu sheet 118 is patterned with a photoresist mask 119 leaving exposed areas 121 corresponding to the thinned regions. The partially-etched Cu sheet 118 is then etched completely through in the exposed areas 121 to form a pattern of holes 116 separating diepad 104a from non-integral pins 104b.

[0015] Fabrication of the QFN package is subsequently completed by affixing the die to the diepad, attaching bond wires between the die and diepad and non-integral pin portions, and then enclosing the structure within plastic encapsulation, as is well known in the art.

[0016] The etching stage of the QFN package fabrication process shown in Figure 1F is relatively difficult to control with precision. Specifically, the accuracy of etching the Cu lead frame in small areas is about 20-25% of the total lead frame thickness. This is due to inability to rapidly and reproducibly halt the progress of chemical etching reaction once it is initiated. Etching outside the above tolerance range can result in the scrapping of many lead frames, elevating package cost.

[0017] Moreover, the conventional approach of partial etching to shape thinned features limits the pitch of the lead, and thus the number of pins available for a given QFN package body size. This limitation in lead pitch results from the at least partially isotropic character of the etching process, which removes material in the lateral, as well as vertical, direction.

[0018] Therefore, there is a need in the art for improved techniques for fabricating semiconductor device packages.

BRIEF SUMMARY OF THE INVENTION

[0019] Embodiments in accordance with the present invention relate to the use of electroplating techniques to form features on the surface of a metal lead frame used in the

packaging of semiconductor devices. In accordance with one embodiment, electroplating is used to fabricate portions of the diepad and of the non-integral pins that are shaped to remain securely encapsulated within the plastic molding of the package. In accordance with another embodiment, electroplating may be used to fabricate protrusions on a package underside which elevate it above the surface of the PC board, thereby preserving the rounded shape of solder balls used to secure the diepad to the PC board. In accordance with yet another embodiment, electroplating may be used to fabricate raised patterns on the upper surface of the diepad for ensuring uniform spreading of adhesive used to secure the die to the diepad, thereby ensuring level attitude of the die within the package.

[0020] An embodiment of a method in accordance with the present invention for fabricating a lead frame for a semiconductor device package, comprises, providing a first metal layer and patterning a mask over the first metal layer to reveal exposed regions. A metal is electroplated in the exposed regions, the mask is removed, and at least a portion of the first metal layer and the electroplated metal are encapsulated within a dielectric material.

[0021] An alternative embodiment of a method in accordance with the present invention for fabricating a lead frame for a semiconductor device package, comprises, providing a first layer, and patterning a first mask over the first layer to reveal first exposed regions. A first metal is electroplated over the first layer in the first exposed regions. A second mask is patterned over the first mask to reveal second exposed regions, and a second metal is electroplated over the first mask in the second exposed regions. The first and second masks are removed, and at least a portion of the first metal and the second metal are encapsulated within dielectric material.

[0022] Another alternative embodiment of a method in accordance with the present invention for fabricating a metal lead frame, comprises, patterning a negative photoresist mask over a substrate, and electroplating raised portions of a copper lead frame within regions exposed by the negative photoresist mask. A positive photoresist mask is patterned over the negative photoresist mask and the raised copper portions. Diepad and pin portions of the copper lead frame are electroplated within regions exposed by the positive photoresist mask. The negative and positive photoresist masks are removed, and

a die is attached to the diepad. The die and lead frame are encapsulated within plastic, and the raised copper portions and the plastic are separated from the substrate.

[0023] An embodiment of a lead frame in accordance with the present invention for a semiconductor device package, comprises, a diepad comprising a metal, and a pin separate from the diepad. An electroplated raised feature comprising the metal is formed on at least one of the diepad and the pin.

[0024] These and other embodiments of the present invention, as well as its features and some potential advantages are described in more detail in conjunction with the text below and attached figures.

BRIEF DESCRIPTION OF THE DRAWINGS

[0025] Figure 1A shows an underside plan view of a conventional QFN package.

[0026] Figure 1B shows a cross-sectional view of the package of Figure 1A taken along line B-B'.

[0027] Figure 1C shows a plan view of the lead frame only, of the conventional package of Figures 1A-B.

[0028] Figure 1D shows a plan view of a copper alloy metal sheet bearing a pattern of holes as is used to fabricate the package of Figures 1A-B.

[0029] Figures 1E-1H show cross-sectional views of specific steps for fabricating the lead frame of Figure 1C.

[0030] Figure 2 shows a flow chart of steps of an embodiment of a process in accordance with the present invention for fabricating a QFN package.

[0031] Figures 3A-E show cross-sectional views of the process for fabricating a QFN package shown in Figure 2.

[0032] Figures 3AA-EA show plan views of the method of Figures 3A-E.

[0033] Figures 4 shows a flow chart of steps of an alternative embodiment of the process in accordance with the present invention for fabricating a QFN package.

[0034] Figures 5A-J show cross-sectional views of the fabrication process shown in Figure 4.

[0035] Figures 5AA-FA show plan views of the process steps shown in Figures 5A-F.

[0036] Figure 6 shows an underside plan view of an alternative embodiment of a package fabricated in accordance with the present invention.

[0037] Figure 7 shows an underside plan view of another alternative embodiment of a package fabricated in accordance with the present invention.

[0038] Figures 7A-H show simplified cross-sectional views of one embodiment of a process in accordance with the present invention for fabricating the package shown in Figure 7.

[0039] Figure 8 shows a cross-sectional view of another embodiment of a package fabricated in accordance with the present invention.

[0040] Figure 9A shows a plan view of a matrix of lead frame designs in accordance with one embodiment of the present invention, secured within a metal frame.

[0041] Figure 9B shows a plan view of a matrix of lead frame designs in accordance with another alternative embodiment of the present invention.

[0042] Figure 9C shows a plan view of a matrix of lead frame designs in accordance with another alternative embodiment of the present invention.

[0043] Figure 10A shows an underside plan view of one embodiment of a package fabricated in accordance with the present invention.

[0044] Figure 10B shows a corresponding cross-sectional view of the package of Figure 10A featuring pins of uniform height.

[0045] Figure 10C shows a corresponding cross-sectional view of the package of Figure 10A featuring taller pins at the outer edge of the package.

[0046] Figure 11 shows a cross-sectional view of another embodiment of a package fabricated in accordance with the present invention.

[0047] Figure 12 shows a cross-sectional view of an alternative embodiment of a package in accordance with the present invention.

[0048] Figure 13A shows a cross-sectional view of another alternative embodiment of a QFN package fabricated in accordance with the present invention.

[0049] Figure 13B shows a plan view of the package shown in Figure 13A.

DETAILED DESCRIPTION OF THE INVENTION

[0050] Embodiments in accordance with the present invention relate to the fabrication of packages for semiconductor devices, and in particular to the use of electroplating techniques to form features on the surface of a metal lead frame. In accordance with one embodiment, electroplating is used to fabricate non-integral pin portions shaped to remain securely encapsulated within the plastic molding of the package. In accordance with another embodiment, electroplating may be used to fabricate protrusions on the underside of the lead frame for elevating the package above the PC board, thereby preserving the rounded shape of solder balls used to secure the diepad to the PC board. In accordance with yet another embodiment, electroplating may be used to fabricate raised patterns on the upper surface of the diepad for ensuring uniform spreading of adhesive used to secure the die to the diepad, thereby ensuring level attitude of the die within the package

[0051] Figure 2 shows a flow chart of the processing steps for fabricating a QFN package in accordance with one embodiment of the present invention. Figures 3A-E show cross-sectional views of the processing steps shown in Figure 2. Figures 3AA-3EA show plan views of the processing steps shown in Figures 3A-E, respectively.

[0052] In first step 202 of process 200 illustrated in Figures 3A and 3AA, Cu roll 300 having a thickness of about 4 mils is provided. The lower surface of Cu roll 300 bears a selectively electroplated layer 302 comprising Ni (0.5-3.0 μm) and Ag (0.5-3.0 μm), or comprising Ni (0.5-3.0 μm)/Pd (~0.15 μm)/Au (0.015 μm). This layer 302 is supported and protected/covered by adhesive tape 303.

[0053] In step 204 illustrated in Figures 3B-BA, the electroplated Cu roll 300 is etched completely through to define a pattern of holes 304 separating diepad 306 from non-integral pins 308. The corresponding plan view shown in Figure 3BA also shows the definition of tie bars 310 and tabs 312 securing diepad 306 and non-integral pins 308, respectively, to surrounding Cu roll 300 during this step.

[0054] Figure 3BA also shows that diepad 306 formed during this step features a periphery 301 exhibiting a serpentine shape. Projections of this serpentine shape 301 serve to lock the diepad into the plastic mold to maintain package integrity under a range of temperature and moisture conditions.

[0055] In step 206 illustrated in Figures 3C-CA, mask 320 of photoresist is patterned to reveal lead-post pin regions 308a and diepad regions 306a desired to have additional thickness.

[0056] In step 208, illustrated in Figures 3D-DA, the exposed regions 306a and 308a are subjected to electroplating conditions to form thickened lead-posts 308b and diepad 306b out of copper material. In accordance with one embodiment of the present invention, Cu material having approximately the same thickness as the original roll may be added during this step by electroplating.

[0057] In step 210 illustrated in Figures 3E-EA, layer 322 comprising Ag/Ni or Au/Pd/Ni is electroplated onto exposed surfaces of lead-post 308 and diepad 306. The mask is then stripped, to reveal electroplated diepad 306 and pins 308 secured to the surrounding Cu roll 300 by tie bars 310 and tabs 312, respectively.

[0058] In steps 212, 214, and 216 of Figure 2, fabrication of the package is completed by inverting the structure, removing the tape, attaching the die to the diepad, connecting bond wires between the die and pins, and encapsulating the entire lead frame/die/bond wire assembly within a molded plastic material. In step 218 of Figure 2, the individual package is then singulated from the surrounding metal frame by physically sawing through the bars and tabs.

[0059] In the first embodiment shown in Figures 3A-EA, regions of additional thickness of the lead frame corresponding to the exposed lead-posts and diepad are formed by the addition of Cu material. Specifically, a layer of Cu material of precise thickness may be deposited by electroplating over the Cu roll under carefully controlled conditions. The precision of this electroplating process is ± 1 μm or less. This precision may be compared with conventional etch processes, which exhibit a precision of ± 25 μm for a Cu substrate having an overall thickness of 4-5 mils. The superior precision of electroplating processes over etching processes may be attributed to the ability to quickly halt electrochemical addition of material reaction by changing the electrical potential.

[0060] The embodiment of the present invention shown in Figures 2, and 3A-EA offer a number of advantages. One advantage is relative similarity to the conventional package fabrication process. Specifically, fabrication is accomplished in part by initially etching a pattern of holes completely through an underlying Cu roll. This similarity allows similar

machinery to be used in fabricating the package, facilitating implementation of the new process flow and reducing the die free package cost (DFAC) in the short term.

[0061] However, one potential drawback of the process flow shown in Figures 2 and 3A-EA, is the continued need to separate the encapsulated package from the surrounding metal frame by physically sawing through the tie bar and tab structures. This singulation by severing of metal connections by sawing is relatively slow and unreliable.

[0062] Accordingly, Figure 4 shows a flow chart of a series of steps, and Figures 5A-K show cross-sectional and plan views of certain steps, for an alternative embodiment of a process in accordance with the present invention for fabricating a QFN package.

[0063] In first step 402 of process 400 illustrated in Figures 5A-AA, a Cu roll 500 having a thickness of about 4 mils is provided. Cu roll 500 may include index holes 501 to indicate positioning.

[0064] In second step 404, as illustrated in Figures 5B-BA, mask 502 comprising negative photoresist material having a thickness of about 100 μm is patterned over Cu roll 500. Openings in this first photoresist mask define the location of lead frame portions of reduced thickness.

[0065] In step 406, as illustrated in Figures 5C-CA, the Cu roll is cleaned, and layer 504 comprising Au/Pd/Ni (total thickness ~ 2.5-3 μm) or Ag/Ni (total thickness 4.5-5.5 μm) is formed by electroplating in regions 502a exposed by mask 502.

[0066] In step 408 as illustrated in Figures 5D-DA, with patterned negative photoresist mask 502 still in place, Cu material 506 is having a thickness of about 100 μm is formed over Au/Pd/Ni or Ag/Ni layer 504 in exposed regions by electroplating. Cu material 506 formed during this step comprises the portions of the non-integral lead frame that will remain exposed following encapsulation.

[0067] In step 410 as illustrated in Figures 5E-EA, positive photoresist mask 508 also having a thickness of about 100 μm is patterned over existing negative photoresist mask 504. The area of regions exposed by positive photoresist mask 508 is larger than the area of regions exposed by first mask. The use of photoresist material of opposite polarity to form the successive masks 504 and 508 is necessitated by the need to develop the second mask without altering the shape of the existing first mask.

[0068] In step 412 as illustrated in Figures 5F-FA, a second Cu layer 510 having a thickness of about 100 μm is then deposited in regions exposed by the second negative mask 508. The Cu material formed during this step comprises the bulk, thick portion of the diepad and non-integral lead portions of the resulting package. Portions of the second deposited Cu layer will form over the underlying positive photoresist through a lateral outgrowth from adjacent copper.

[0069] In step 414 illustrated in Figure 5G, an Ag layer 512 is deposited by electroplating over the second Cu layer 510 in regions exposed by the second photoresist mask. This selective deposition to form Ag can utilize a mask (not shown).

[0070] In step 416 illustrated in Figure 5H, the first and second patterned photoresist masks are stripped. At this stage in the fabrication process, and in contrast with the conventional QFN fabrication approach and with the first embodiment, the diepad and non-integral lead portions are not secured to a surrounding metal frame by tabs or tie bars. Rather, these components are secured in place by contact with the underlying Cu roll substrate.

[0071] Owing to this absence of the tie bars, the lead frame of this second embodiment includes four additional pins. These additional pins are located in regions formerly occupied by the tie bars.

[0072] In step 418 illustrated in Figure 5I, die 550 is attached to the diepad portion with electrically conducting adhesive, and bond wires 552 are connected between die 550 and the pins. In step 420 illustrated in Figure 5J, the die/lead frame combination is encapsulated in plastic material 556 while still being supported by the Cu roll 500.

[0073] In step 422 illustrated in Figure 5K, an array of packages within the encapsulant are separated from the underlying Cu support roll by selective chemical etching. A number of Cu etching techniques are known in the art. One approach involves exposure to aqueous $FeCl_3$, and is described in detail by Duffek and Armstrong, "Etching in Printed Circuit Handbook" - Chapter 6, C.F. Coombs, Ed. (McGraw-Hill, New York, 1967). Another approach involves exposure to a known Cu electroplating solution, reversing the electroplating process to remove Cu. This latter approach is described by Parthasaradhy, "Practical Electroplating Handbook (Prentice Hall, Englewood Cliffs, NJ, 1989). Both of the above-cited references are incorporated by reference herein for all purposes.

[0074] After the separation step of Figure 5K, individual QFN packages are singulated from the array by sawing through the mold only. The softness of the plastic encapsulant as compared with the metal, allows the singulation process to occur more easily and with fewer defects.

[0075] Moreover, in accordance with still other embodiments of the present invention, mold for the plastic encapsulant may be designed such that each QFN is individually molded within discrete cavities or cells of the mold, with the QFN units held together by contact with the common substrate carrier roll. Using such a specially designed mold, the individual QFN packages could be singulated entirely by chemical exposure, without any need for physical separation by sawing. This approach may reduce lead frame density by including a honeycomb of walls defining cells within the mold, but would avoid the difficult sawing step.

[0076] The embodiment shown in Figures 4 and 5A-5K offers the advantage of not requiring sawing or otherwise physically severing connections between copper pieces to singulate individual packages. Rather, this package singulation process takes place by way of chemical exposure. The efficiency of this chemical-singulation process reduces the DFPC in the long term. The QFN process flow given in Figure 4 also allows strip testing of the packages, because the removal of the packages from the substrate by chemical activity results in separation of the leads.

[0077] While some of the embodiments of the present invention have been described herein, it should be understood that these are presented by way of example only, and these descriptions are not intended to limit the scope of this invention.

[0078] For example, while the specific embodiment for forming a QFN package illustrated in Figures 4 and 5A-K utilize a copper roll as the underlying substrate upon which features of the lead frame are successively electroplated, this is not required. In still other alternate embodiments in accordance with the present invention, lead frame features could be formed by successive electrodeposition steps performed on substrates other than copper, for example steel..

[0079] While the previous discussion has focused upon fabrication of a particular type of QFN package, embodiments in accordance with the present invention are not limited to fabricating any specific package. For example, the present invention does not require fabrication of a package having any particular number of pins. Figure 6 shows a plan

view of another alternative embodiment of a QFN package 604 having a lead frame fabricated in accordance with the present invention with only eight pins 608.

[0080] And while the previous discussion has focused upon QFN packages having a single bank of non-integral pins adjacent to the diepad, the present invention is not limited to this particular configuration. Figure 10A shows a plan view of the underside of QFN package 1050 having an inner bank 1052 and an outer bank 1054 of exposed pin structures 1056. Figure 10B shows a corresponding simplified cross-sectional view of one embodiment of the package shown in Figure 10A, featuring pins banks 1052 and 1054 having the same height.

[0081] Figure 10C shows a cross-sectional view of an alternative embodiment of the package of Figure 10A. Package 1000 shown in Figure 10C features outer bank 1054 comprising pins at the outer edge of the package that are taller than the pins of the inner bank 1052. The different height of pin banks of the specific package shown in Figure 10C aids in preventing physical interference between bond wires connecting the pins with the central die. The package of Figure 10C could be fabricated by electroplating in accordance with embodiments of the present invention utilizing more than two masks. The particular embodiment shown in Figure 10C also enables wire-bonding to replace Ball Grid Array (BGA) with an interposer structure, in packages featuring a medium pin count, reducing package cost.

[0082] Furthermore, in packages having a high pin count, the exposure of the diepad on the underside of the package may be undesirable. In such package designs where exposure of the lead frame is to be avoided, the conventional fabrication approach involves partial etching of the diepad to reduce its thickness. Such a partial etching step, however, suffers from the lack of precision and additional expense described above.

[0083] In accordance with embodiments of the present invention, however, a package having a non-exposed diepad can be fabricated by electrochemical deposition on an underlying substrate. Figure 7 shows a simplified plan view of such a QFN package 700, wherein pins/lead posts 702 are exposed on underside surface 700a, but the diepad is not.

[0084] Figures 7A-H show simplified cross-sectional views of one embodiment of a process for fabricating the package shown in Figure 7. In Figure 7A, a first silver layer 710 is selectively formed by masked electrode position over an underlying metal substrate

712. In this step, Ag is formed only in regions corresponding to the position of exposed lead posts or pins.

[0085] In Figure 7B, a positive photoresist mask 714 is patterned over substrate 712, such that exposed regions correspond to existing Ag layer, and exposed regions correspond to the expected outline of the diepad. Also shown in Figure 7B, a first Cu layer 716 is formed within the exposed regions 715. Further shown in Figure 7B, Au/Pd/Ni layer 718 is also deposited within regions exposed by positive photoresist mask 714. As described in detail below, the copper deposited in exposed region during this step is sacrificial, and will later be removed by etching to the Ag/Pd/Ni layer 718, which serves as an etch stop.

[0086] In Figure 7C, a negative photoresist mask 720 is patterned over positive photoresist mask 714. Also shown in Figure 7C, a second Cu layer 722 is deposited by electroplating in regions by negative photoresist mask 720.

[0087] Figure 7D shows formation of a second silver layer 724 by masked electrodeposition over second Cu layer 722. Figure 7E shows the removal of the photoresist masks to define lead frame 731 comprising diepad 752 and separate lead posts/pins 732, supported on underlying substrate 712.

[0088] Figure 7F shows the subsequent package fabrication steps of attaching die 750 to diepad 752, and attaching bondwires 756 between die 750 and diepad 752 and pins 758. The die/lead frame combination is then enclosed within plastic encapsulant 760.

[0089] Figure 7G shows removal of the encapsulated package 762 from the underlying substrate by chemical exposure.

[0090] Figure 7H shows subsequent inversion of the encapsulated package 762, followed by etching of exposed Cu material to create cavity 764 in the underside of the package. Ag/Pd/Ni layer 718 serves as an etch stop during this process.

[0091] In subsequent fabrication steps (not shown), cavity 764 is filled in with additional plastic material. During this second molding process, the additional plastic material may also cover the exposed pins/lead posts. In such case, the pins/lead posts can be re-exposed by chemical-mechanical planarization of the package underside.

[0092] As previously described in connection with the first embodiment, raised features may formed by electroplating additional Cu material over an existing Cu roll. This Cu roll may be patterned with holes by etching or punching to define a matrix of proto-diepad and pin regions secured to the surrounding metal frame by tabs and tie-bars. However, embodiments in accordance with the present invention are not limited to fabricating any particular matrix of framed structures. Figures 9A-C show plan views of different matrices of lead frame designs which may be fabricated utilizing the present invention.

[0093] While the above referenced discussion has focused upon electroplating techniques to form continued pin structures conducive to physical retention within the plastic package, the present invention is not limited to forming this type of raised feature. Alternative embodiments in accordance with the present invention utilize deposition by electroplating to fabricate other raised features.

[0094] For example, Figure 8 shows a cross-sectional view of one alternative embodiment of a package in accordance with the present invention. Power ball grid away (BGA) package 800 of Figure 8 features die 802 secured to the underside of diepad 804 and between projecting metal pin portions 806. Package 800 is secured to PC board 808 by solder balls 810. Unlike the QFN and other package types discussed herein, the pins of the power BGA package are not encapsulated within a plastic material.

[0095] Studs 812 protruding from pins 806 make contact with the underlying traces on the PC board. The presence of studs 806 raises the lower surface of the package off the surface of the PC board, thereby allowing solder balls 810 to maintain their rounded shape when the package is secured to the PC board. The Cu studs are about 6-10 mils in diameter and are covered by Ni/Pd/Au or Ni/Ag deposited layers for solderability and protection of the solderable layer (Ni).

[0096] Maintaining the rounded shape of the solder balls is beneficial by allowing removal and reworking of soldered packages. The raised stud features of the power BGA package shown in Figure 8 may be selectively deposited on the exposed pins utilizing masked electroplating techniques according to the present invention.

[0097] Embodiments in accordance with the present invention are also suited for fabricating QFN packages which utilize aspects of the ball grid array architecture shown in Figure 8. For example, Figure 11 shows a simplified cross-sectional view of another alternative embodiment of a package fabricated in accordance with the present invention.

[0098] Package 1100 comprises die 1102 supported on lead frame 1104 having raised projections 1106 on the underside. The package 1100 of Figure 11 thus allows only selected portions of the diepad 1104 to be exposed on the underside of the package. The package type shown in Figure 11 allows solder balls of the same size to be used to attach all exposed pins and die pads, facilitating manufacture in a manner compatible with conventional BGA-type manufacturing processes.

[0099] Figure 12 shows a simplified cross-sectional view of yet another alternative embodiment of a package in accordance with the present invention. Diepad 1200 of package 1202 comprises a number of individual, non-integral pins 1204 in electrical communication with corresponding contacts on the underside of die 1206 through internal solder connections 1208. Pins 1204 are securely embedded within plastic encapsulant 1210 by virtue of the presence of raised portions 1204a selectively deposited utilizing electroplating techniques according to embodiments of the present invention. Pins 1204a are in electrical communication with, and physically supported by, PC board 1212.

[0100] Package 1202 offers a small, thin housing for integrated circuits (ICs) featuring multiple pads. Such a package, commonly referred to as a Chip Scale Package (CSP), may be fabricated using solder ball connections between IC chip pads and pins formed by electrodeposition in accordance with embodiments of the present invention. Such CSP packages can be attached to the PC board using solder balls or surface mount die attach processes.

[0101] Figure 13A shows a cross-sectional view, and Figure 13B shows an underside plan view, of yet another embodiment of the QFN package design that may be fabricated in accordance with embodiments of the present invention. Package 1300 of Figure 13 is similar to that shown in Figures 3A-3EA, except that the top surface of the diepad portion 1302 now bears raised waffle pattern 1304 having a thickness of between about 1.5-2 mil and a diameter of between about 4-10 mils. The exposed surfaces of these raised waffle patterns may, but need not, be covered with Ag/Ni or Au/Pd/Ni electroplated films.

[0102] Raised waffle pattern 1304 serves to compartmentalize conducting adhesive 1306 during spreading as die 1308 being placed on the diepad. Raised waffle pattern 1304 deposited by electroplating in accordance with embodiments of the present invention, can serve to cause the adhesive to be of relatively uniform thickness, ensuring the level attitude of the die within the plastic encapsulation.

[0103] While the embodiment shown and discussed in connection with Figures 13A-B utilize raised features in the form of a continuous waffle pattern, embodiments in accordance with the present invention are not limited to this particular pattern. In accordance with alternative embodiments, the upper surface of a diepad could feature a non-continuous pattern of raised studs to achieve the same purpose. Such raised waffle or stud patterns created in accordance with embodiments of the present invention may be useful for QFN packages as well as other package types, including but not limited to DPAK, D2PAK, TO-220, TO-247, SOT-223, TSSOP-x, SO-x, SSOP-x, and TQFP.

[0104] While the above is a full description of the specific embodiments, various modifications, alternative constructions and equivalents may be used. Therefore, the above description and illustrations should not be taken as limiting the scope of the present invention which is defined by the appended claims.